

An Overview of On-Chip Sensing and Analytics for Resilient Integrated Circuits

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Abstract – Resilient integrated circuits (ICs) are essential for safety- and mission-critical applications, where hardware faults can result in costly damage or even loss of lives. A resilient IC is designed to detect, tolerate, and adapt in real time to different faulty scenarios, maintaining correct functionality under varying operating and environmental conditions. Specialized sensing and analytics engines embedded in the chip play a central role in resilient ICs by providing real-time insight into the overall state, i.e., “health”, of the chip. This paper presents an overview of commonly used on-chip sensors for IC status monitoring, and discusses fundamental design requirements for on-chip processing of sensor-generated data.

Keywords – Resilient integrated circuits, on-chip sensors, self-awareness, self-adaptivity

I. INTRODUCTION

The increasing complexity and miniaturization of integrated circuits (ICs) have led to significant challenges in ensuring reliable system operation. Modern nanoscale ICs are susceptible to a wide variety of transient and permanent faults, which can compromise functionality and reduce system lifetime. These faults are posing serious operational risks in safety- and mission-critical applications, such as automotive, medicine and aerospace.

Traditional design approaches for reliable ICs are based on static redundancy, which is not optimal for dynamic operational environments (e.g., space) and variable application requirements. Moreover, many faults that occur during chip lifetime may not be predicted in the design phase. For example, in 2021, researchers at both Facebook and Google published studies on chip failures whose causes have been hard to identify [1]. As they stated, the problem was not in the software, but in the computer hardware.

In order to address the complex reliability mechanisms, advanced ICs for reliability-critical applications should not

just be reliable, but rather resilient. A resilient IC is capable of detecting faults and even predicting unexpected faults, as well as adapting to faulty scenarios in order to mitigate their impact. In other words, a resilient IC should be self-aware and self-adaptive [2, 3]. Self-awareness is achieved with on-chip sensors for real-time monitoring of vital status parameters. The information from sensors is processed to evaluate the overall system “health”. Finally, based on the health status, the IC may automatically adapt (reconfigure) its architecture to maintain the predefined functionality.

Resilient ICs offer substantial benefits, particularly in terms of reduced maintenance costs and reduced electronic waste through extended chip lifetime. Ultimately, resilient electronics could be the key enabler for long-term deep space missions, paving the way for sustainable human life beyond Earth. However, design of resilient electronics is still faced with numerous technical challenges. Design of resilient ICs requires low-overhead cross-layer sensing and analytics infrastructures, as well as scalable self-adaptation mechanisms that can operate reliably across different operating conditions and system architectures.

In this paper, we present an overview of digital on-chip sensors for IC status monitoring, and discuss the key design requirements for on-chip analytics. The rest of the paper is organized into five sections. In Section II, the basics of hardware faults is introduced. Section III presents the common on-chip sensors. In Section IV, the processing of sensor data is discussed. Section V introduces a design of a resilient processing system for the next generation (6G) wireless communication networks, as a typical use case for resilient ICs. The paper is concluded in Section VI.

II. BASICS OF HARDWARE FAULTS

Hardware faults (transient and permanent) in ICs may originate from external sources (e.g., ionizing radiation, electromagnetic noise) or from various on-chip imperfections (gradual component aging, manufacturing defects).

Transient faults do not physically damage the device, but they can cause unrecoverable data corruption, system crashes, and functional malfunctions. The most prevalent transient faults are soft errors [4], i.e., bit-flips in memory elements and sequential logic. Soft errors are typically caused by cosmic radiation, Electromagnetic Interference (EMI), and crosstalk. Under ionizing radiation, soft errors

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arise from Single Event Upsets (SEUs) and Single Event Transients (SETs) caused by energetic particles (e.g., heavy ions, neutrons, and protons). Historically, soft errors have been a primary concern in radiation environments such as space. However, with technology scaling, soft errors have become critical also for mainstream terrestrial electronics such as automotive. Due to technology downscaling and growing design complexity, the chip-level Soft Error Rate (SER) has increased by roughly an order of magnitude from 180 nm to 10 nm technology node [5].

Permanent faults, on the other hand, cause irreversible degradation of device and circuit behavior. They typically originate from manufacturing defects, such as stuck-at, bridging or open-circuit faults, and from aging mechanisms during in-field operation. Aging can result from radiation-induced Total Ionizing Dose (TID) effects or stress-related phenomena, such as Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), Time-Dependent Dielectric Breakdown (TDDB), and electromigration. The aging mechanisms shift transistor threshold voltages and increase leakage currents, ultimately slowing down signal propagation and potentially leading to functional failures. Stress-induced circuit aging has become a major reliability concern in technologies below 45 nm [6].

Susceptibility of an IC to transient and permanent faults is dependent on operating conditions, such as supply voltage, temperature, and clock frequency. Temperature variations can increase the SER of combinational logic at least 2x [7], while supply voltage fluctuations can cause SER variations exceeding 150% [8]. Additionally, the SER due to SETs in combinational logic has been shown to grow linearly with clock frequency [9].

In practical scenarios, different fault mechanisms often interact, giving rise to combined fault effects. For example, both elevated temperature and increased supply voltage lead to accelerated circuit aging. On the other hand, device aging may further increase the susceptibility to soft errors, while reduced supply voltage increases the likelihood of both particle-induced soft errors and timing violations. Moreover, in a real application, an IC is often subjected to a simultaneous impact of different fault types and sources. For example, in space, electronic systems are exposed to both high temperatures and ionizing radiation, while automotive electronics is affected by vibration, electrical stress and elevated temperatures.

III. COMMON DIGITAL ON-CHIP SENSORS FOR IC STATUS MONITORING

On-chip sensors (also referred to as monitors, checkers or instruments) are embedded circuits that monitor different status parameters within an IC. They enable detection of transient and permanent faults in the system, as well as real-time measurement of operational parameters that affect the system reliability, such as supply voltage and current, power consumption, temperature, workload of individual functional units, clock frequency.

Sensor readings are collected and stored in on-chip or off-chip memory, and then analysed to determine the health state of the system. Data generated by sensors could be processed on the chip by customized processing units, or sent to external processing platforms. This processed information allows for the real-time decision-making, such as triggering adaptive voltage scaling, dynamic power management, or adaptive fault tolerance.

In general, on-chip sensors are distributed across the chip and different types of sensors can be applied on the same chip. The sensors can be designed as digital or analog circuits. Analog sensing typically requires analog-to-digital conversion, which adds to the complexity and cost of the design. On the other hand, digital on-chip sensors could be designed with standard or customized combinational and sequential cells. Aiming for efficient and low-cost on-chip solutions, this section gives an overview of common digital on-chip sensors.

A. Soft Error Detectors

Given the criticality of soft errors, detection of bit-flips in storage elements is mandatory for a resilient IC. A wide range of soft error detection techniques has been proposed, and the selection of an optimal solution depends on the target application, performance constraints, and acceptable overheads in terms of area, power, and latency. In practice, an IC may integrate different types of soft error detectors, each tailored to a specific subsystem.

Memory structures are among the most critical components in modern ICs, as memory occupies a large portion of chip area (typically over 50%). A widely used approach for soft error detection in memory combines periodic memory scrubbing with Error Detection and Correction (EDAC) codes, as depicted in Figure 1. Memory scrubbing reads and refreshes stored data at regular intervals, while EDAC schemes provide continuous on-the-fly correction of bit-flips in individual memory locations. EDAC schemes can range from simple Single Error Correction and Double Error Detection (SEC-DED) to more advanced multi-bit error correction codes.

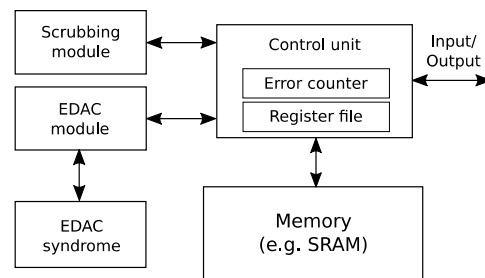


Figure 1: Scrubbing and EDAC for memory

In addition to memory, soft error detection should be applied to processing logic, particularly in control paths and safety-critical datapaths. One of the most effective error detection techniques is duplication with comparison,

where the target circuit is implemented twice and the corresponding primary outputs of the two circuit copies are continuously compared. Any discrepancy between the circuits' outputs is interpreted as an error. More generally, for N copies of the target circuit, voting circuits can be used to flag an error whenever a mismatch between the monitored signals is detected [10]. This approach enables also to detect permanent errors, as any uncorrectable errors can be considered as permanent errors.

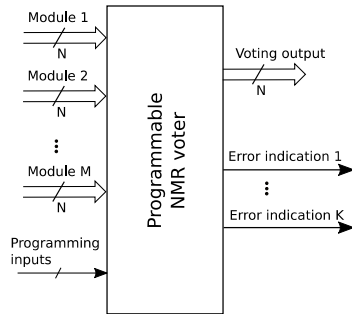


Figure 2: Programmable voter as fault detector

B. Glitch Detectors

Short voltage glitches, such as SETs, may cause data corruption if they propagate through the circuit and are captured by flip-flops. Glitches are especially critical if they occur in control lines (clock, reset), as this may result in system failure. The common approach for mitigating on-chip voltage glitches is by inserting specially designed filtering elements to suppress all glitches shorter than the predefined pulse width. However, it is also important to detect and keep the record of these glitches, as this can help in preventing soft error occurrence.

For detection of voltage glitches, various solutions have been proposed [11, 12]. An approach that provides both glitch filtering and detection is depicted in Figure 3 [13]. Glitch filtering is achieved with a delay line and a guard gate, where the delay line determines the pulse width that can be filtered. Counters are used to capture the occurrence of glitches. One counter captures all pulses (normal pulses and glitches), while the other captures only the normal pulses. Thus, comparing the readings of the two counters enables to determine the number of glitches. To ensure fault-tolerance, counters are designed as self-checking.

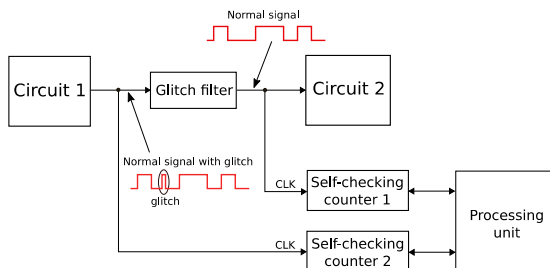


Figure 3: Glitch filter and detector

C. Radiation Detectors

Besides monitoring the state of on-chip circuitry, it may also be necessary to monitor environmental conditions that could result in faults. For example, in space applications, high energy particles emitted during Solar Particle Events (SPEs) are the main cause of soft errors. During an SPE, the particle flux may increase several orders of magnitude, resulting in several orders of magnitude higher SER. Thus, monitoring the particle flux is essential for timely activation of dynamic fault tolerance mechanisms before the actual soft errors occur in the chip.

A wide variety of both off-chip and on-chip solutions for detecting radiation particles are available. Radiation detectors either measure the change of electrical parameters due to radiation exposure, or the number of events caused by radiation (e.g., number of radiation-induced pulses). Common examples are PMOS-based radiation sensors, diode-based radiation sensors and SRAM-based radiation sensors. Other solutions include custom-sized inverter chains, bulk built-in current sensors, and acoustic wave detectors. Each detector has advantages and disadvantages. Therefore, optimal choice for a given design depends on application requirements. Comparative analysis of various radiation detectors, addressing their major strengths and limitations, is given in [14].

D. Aging Monitors

Aging monitoring is essential for tracking the gradual degradation of transistors caused by stress-induced effects. Various implementations of aging sensors exist, where the most common are based on shadow flip-flops and ring oscillators [15, 16]. The real-time insight into circuit aging enables to apply adaptive compensation techniques such as dynamic voltage scaling, body bias adjustments, or workload redistribution, helping to maintain performance and extend the operational lifetime of the system.

One implementation of aging sensor is illustrated in Figure 4. The sensor consists of two flip-flops and an XOR gate, and it is inserted between the input and output of the flip-flop at the end of a critical path. This sensor can also detect soft errors. Three clock signals (Clock 1, Clock 2 and Clock 3) are used for controlling the sensor operation, i.e., selection between aging and soft error detection modes. Detailed description of the sensor operation can be found in [17].

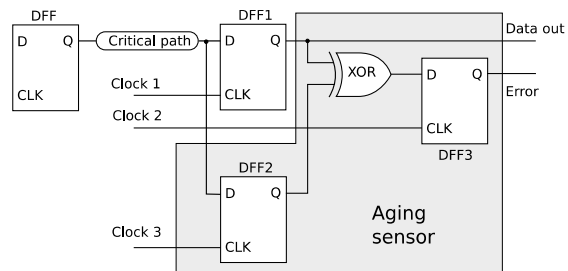


Figure 4: Aging sensor inserted in a critical path

E. Workload Monitors

Workload monitors (also referred to as performance or activity monitors) are used to track the switching activity of individual functional units within an IC, thus providing real-time insight into the dynamic workload distribution across the chip. This information is crucial for assessing the overall aging and power consumption of the circuit, and it could be used as a guide for adaptive power management strategies, such as Dynamic Voltage and Frequency Scaling (DVFS), task migration, and thermal balancing.

A typical implementation of a workload monitor is based on event counters connected to the primary inputs of critical functional units (e.g., enable and clock inputs), as illustrated in Figure 5. The number of detected events (counts) is proportional to the activity of the unit, and directly determines the power consumption of the unit. In addition, this information also gives an insight into the dynamic stress of the unit. More detailed discussion on the design and operation of workload monitors can be found in [18].

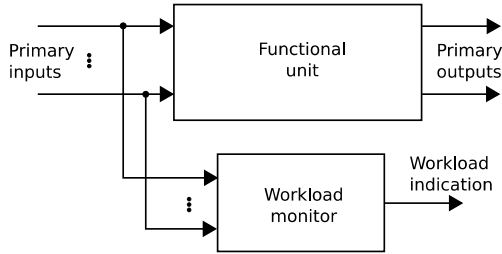


Figure 5: Workload monitor connected to a target functional unit

F. Temperature and Supply Voltage Monitors

Variations in on-chip temperature and supply voltage may significantly affect the overall system performance and reliability. Therefore, continuous monitoring of supply voltage and temperature is essential for detecting abnormal operating conditions and enabling timely actions to preserve the required functionality.

Monitoring of on-chip temperature fluctuations is crucial in preventing excessive localized hotspots. Temperature information enables dynamic thermal management techniques such as DVFS, adaptive body biasing, and workload migration. In parallel, continuous monitoring of supply voltage levels is essential for effective power management and mitigating aging effects. Thus, combined monitoring of temperature and supply voltage enables the system to balance performance, energy efficiency, and reliability under varying operating conditions.

The simplest and most common digital implementation of temperature and supply voltage sensors is based on ring oscillators [19], as the frequency of ring oscillator depends on both temperature and supply voltage. However, in this case, it is important to differentiate between the impact of temperature and supply voltage. One solution is to use two or more ring oscillators designed with different temperature and voltage sensitivities and solving a calibrated system of

equations based on their measured frequencies.

An architecture of a temperature and/or supply voltage monitor with two ring oscillators is depicted in Figure 6. The operating principle is based on measuring the number of oscillations (by the asynchronous counter) in a given time interval (defined by the timer). Besides simultaneous measurement of temperature and supply voltage, the use of two ring oscillators provides inherent redundancy, ensuring that the sensor remains functional if one oscillator fails.

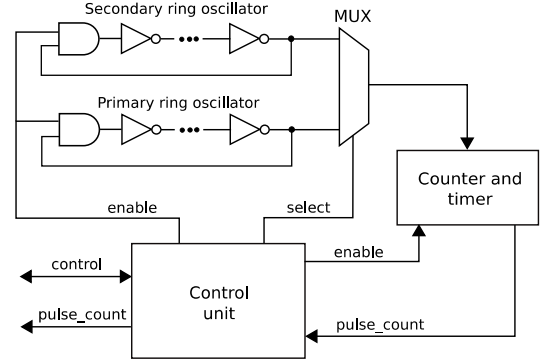


Figure 6: Temperature and/or supply voltage monitor based on ring oscillator

IV. COLLECTION AND PROCESSING OF DATA FROM ON-CHIP SENSORS

In order to assess the overall health of the system, data from sensors should be continuously collected, stored in a memory, and then periodically processed. A history of all sensor readings is required for accurate assessment of the system health and prediction of possible failures. Predictive capabilities are especially important in space missions, where prediction of SPEs before they occur enables to activate preemptive protection measures. Our prior work [20] has proposed a machine learning accelerator for SPE prediction using on-chip SRAM as a particle detector.

Processing of sensor data on the chip can be implemented either in hardware (with a dedicated hardware accelerator) or in software program executed by a general purpose processor. Rule-based decision making is the basic processing approach that could be applied. For example, if certain monitored parameter reaches a predefined threshold level, appropriate action could be initiated. Alternatively, when complex dependencies have to be taken in account, machine learning algorithms could be applied.

An important goal in the design of on-chip sensing and analytics engine is to minimize the overhead in terms of area and power consumption. Typical area/power overhead due to on-chip sensors and corresponding processing logic should not exceed 10-15%. To minimize area overhead, sensors should be placed only in the most critical spots. To minimize power consumption, shut-down functionality is applied to all sensors that do not have to be continuously active (e.g., aging and temperature sensors).

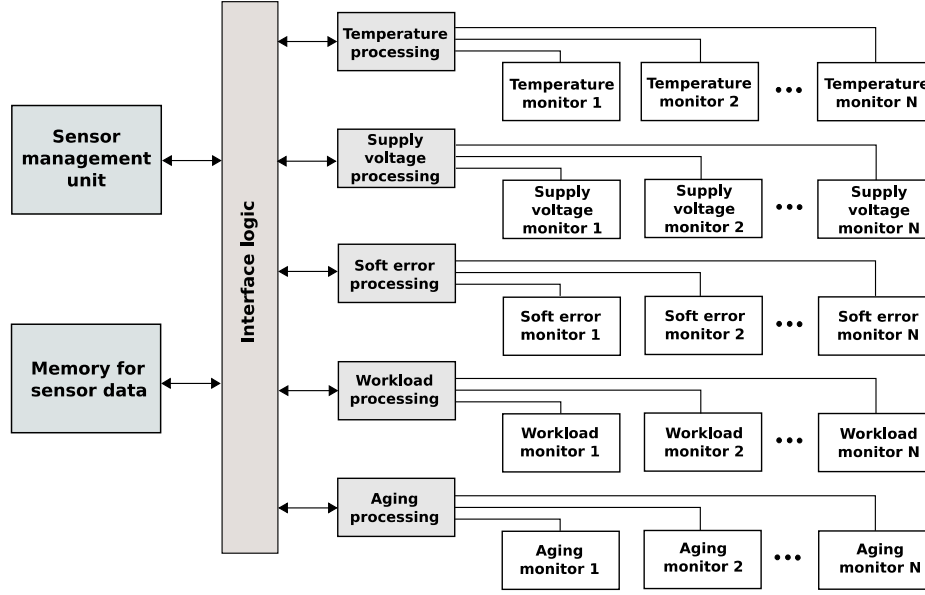


Figure 7: General concept of on-chip sensing and analytics architecture

A general architecture of on-chip sensing and analytics engine is illustrated in Figure 7. Besides on-chip sensors, the engine consists of the following functional units:

- **Processing Units:** A dedicated processing unit is allocated for each type of sensor. It collects data from the corresponding sensors and performs initial processing and formatting of sensor readings.
- **Memory:** The history of sensor readings is stored in a non-volatile memory, which could be integrated on the chip or placed externally.
- **Sensor Management Unit:** It controls the transfer of data from processing units to the memory, and periodically processes the information stored in memory in order to assess the chip's health. It can also predict potential faulty scenarios using machine learning algorithms trained during the design phase.
- **Interface:** The on-chip sensing and analytics logic should ideally cause no interference with the main system. To reduce this possibility, it must be ensured that sensors and processing logic use separate communication buses, and not the main communication bus used by the system.

All above mentioned units should be designed to be fault-tolerant. The sensors should also be fault-tolerant or fault-aware in order to avoid false readings. Based on the estimated system health, specially designed reconfiguration unit may perform the required adaptations to improve the system resilience and maintain the required functionality. For example, the reconfiguration unit may adjust supply voltage or frequency, switch off certain functional units to reduce power supply, or activate N-Modular Redundancy to improve system reliability.

V. CASE STUDY: A RESILIENT PROCESSING PLATFORM FOR 6G WIRELESS COMMUNICATIONS

Resilient hardware components will be essential for the next generation (6G) wireless communication networks, particularly for the 3D networks aimed to integrate ground, aerial and space communication segments. To this end, we have designed a prototype of a resilient processing platform for joint communication and sensing in 6G networks. The platform combines quad-core RISC-V-based processor and triple-core accelerators, as illustrated in Figure 8.

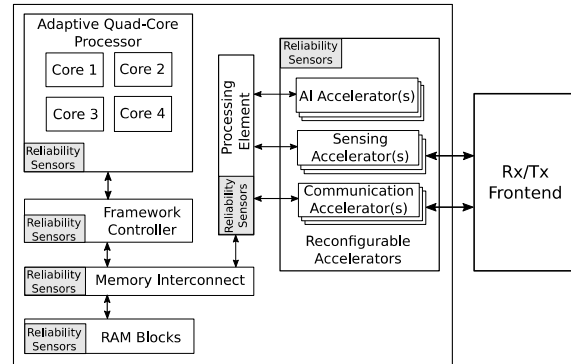


Figure 8: Resilient processing platform for 6G networks

The quad-core processor is an upgrade of our TETRISC system [21], which is based on the single-core platform PULPissimo [22]. Besides processor, important components are the hardware accelerators. The AI accelerator is a multi-modal, multi-tasking Convolutional Neural Network

(CNN) accelerator for classification of radar images. The sensing accelerator is intended for preliminary processing of data from radar. The communication accelerator acts as an interface towards the communication system. All three accelerators are designed as triple-core to support multiple operating modes.

In the initial version of the processing platform, three operating modes for quad-core processor and triple-core accelerators are supported:

- *High-performance mode*: All cores are working in parallel, executing their own tasks.
- *Fault-tolerant mode*: Cores operate in Dual Modular Redundancy (DMR) or Triple Modular Redundancy (TMR) configurations to enhance fault tolerance.
- *Low power mode*: One or more cores are switched off to reduce power supply and aging.

The operating modes are selected by the Framework Controller, a custom-designed unit for storing and processing the data from on-chip sensors. More details on the processing platform can be found in [21, 23, 24]. After initial implementation on a commercial FPGA, future work will be focused on ASIC implementation and testing under realistic use case scenarios.

VI. CONCLUSION

This work presents an overview of on-chip sensors for monitoring the system status and detection of hardware faults in resilient ICs. The most common digital sensors are presented, and a design concept for processing of sensor data is discussed. As case study, a resilient processing platform for joint communication and sensing in 6G wireless communication networks is proposed.

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